AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A non-volatile programmable memory cell formed in a p-type semiconductor substrate and useful in a memory array having column bitlines and row wordlines, the memory cell comprising:

a transistor having a p+ doped gate, a gate dielectric between the gate and over said substrate, and first and second doped semiconductor regions formed in said substrate adjacent said gate and in a spaced apart relationship to define a channel region therebetween and under said gate, the gate being formed from one of said column bitlines; and

wherein the second p+ doped semiconductor region of the transistor is connected to one of said row wordlines, and wherein said row wordline is formed by an n-type region near the surface of said semiconductor substrate.

2. (Original) The memory cell of Claim 1 wherein said gate is formed from one of said column bitlines.

3. (Currently Amended) The memory cell of Claim 1 wherein said memory cells further including a non-volatilely programmed doped region formed in said substrate in a channel region when said memory cell has been programmed.

4. (Currently Amended) A non-volatile programmable memory cell formed in an n-type well and useful in a memory array having column bitlines and row wordlines, the memory cell comprising:

a transistor having a n+ doped gate, a gate dielectric between the gate and over a substrate, and first and second doped semiconductor regions formed in said substrate adjacent said gate and in a spaced apart relationship to define a

channel region therebetween and under said gate, the gate being formed from one of said column bitlines; and

wherein the second n+ doped semiconductor region of the transistor is connected to one of said row wordlines, and wherein said row wordline is formed by a p-type region near the surface of said n-type well.

5. (Original) The memory cell of Claim 4 wherein said gate is formed from one of said column bitlines.

6. (Currently Amended) The memory cell of Claim 4 wherein said memory cells further including a non-volatilely programmed doped region formed in said substrate in a channel region when said memory cell has been programmed.

7. (Original) The memory cell of Claim 4 wherein said n-type well is replaced by an n-type substrate.

8-14. (Cancelled)